CLAIMS:

1. A high speed bit stream data conversion circuit comprising:

a first plurality of input ports that receive a first plurality of bit streams at a first bit rate;

a plurality of data conversion circuits that receive the first plurality of bit streams and that produce at least one second bit stream at a second bit rate, wherein the number and bit rate of the first plurality of bit streams and the at least one second bit stream differ;

a plurality of symmetrical data circuit pathways that comprise pairs of circuit pathways, and that transport the first plurality of bit streams from the first plurality of input ports, and to the plurality of data conversion circuits, wherein a transmission time for the first plurality of bit streams on the plurality of symmetrical data circuit pathways are substantially equal;

a clock distribution circuit that receives a data clock signal at a clock port located at a midpoint of the first plurality of input ports, and symmetrically distributes the data clock signal to the plurality of data conversion circuits along a plurality of symmetrical clock circuit pathways, wherein the symmetrical pathways further comprise a central trunk coupled to the clock port and wherein the trunk is located between a first pair of circuit pathways, and symmetrical pairs of branches that extend from the trunk and couple to the data conversion circuits, and wherein the clock transmission times associated with each symmetrical clock circuit pathway are substantially equal, and wherein the distributed data clock signal latches data in the data conversion circuits from

the first plurality of bit streams to the second plurality of bit streams, and wherein the pairs of circuit pathways comprise a first pathway located on a first side of the trunk and a second pathway located on a second side of the trunk, wherein the second side is opposite the first side.

2. The high speed bit stream data conversion circuit of Claim 1, wherein the clock distribution circuit further comprises a plurality of delay elements operable to compensate for skewing of the data clock signal received by each data conversion circuit.

3. The high speed bit stream data conversion circuit of Claim 2, wherein the delay elements comprise switched capacitor networks that introduce delay increments based on a capacitance coupled to a buffer amplifier.

4. The high speed bit stream data conversion circuit of Claim 3, wherein the capacitance coupled to the buffer amplifier is a variable capacitance.

5. The high speed bit stream data conversion circuit of Claim 4, wherein the variable capacitance will increase or decrease the buffer amplifier delay time.

6. The high speed bit stream data conversion circuit of Claim 1, wherein the plurality of symmetrical data circuit pathways that transport the first plurality of bit streams are symmetrical with respect to the symmetrical clock circuit pathways.

7. The high speed bit stream data conversion circuit of Claim 2, wherein each symmetrical data circuit pathway that transports the first plurality of bit streams further comprises a retimer that ensures data integrity between the first plurality of bit streams and the at least one second bit.

8. The high speed bit stream data conversion circuit of Claim 7, wherein the data conversion circuit comprises a multiplexer, wherein a number of first bit streams exceeds a number of second bit streams, and wherein the second bit rate exceeds the first bit rate.

9. The high speed bit stream data conversion circuit of Claim 8, wherein the plurality of first bit streams comprise 4 bit streams at a bit rate of about 10GBPS, and wherein the at least one second bit stream comprises 1 bit stream at a bit rate of about 40 GBPS.

10. The high speed bit stream data conversion circuit of Claim 8, wherein the first plurality of bit streams comprise 16 bit streams at a bit rate of about 2.5 GBPS, and wherein the at least one second bit streams comprise 4 bit stream at about 10 GBPS.

11. The high speed bit stream data conversion circuit of Claim 1, wherein a physical length of each symmetrical data circuit pathways is substantially equal, and wherein a physical length of each symmetrical clock circuit pathways is substantially equal.

12. A method of converting high speed data bit streams from a first bit rate to a second data, wherein the first and second data rate differ, comprising the steps of:

receiving a first plurality of bit streams at a first plurality of input ports;

distributing the first plurality of bit streams to a plurality of data conversion circuits along a plurality of symmetrical data circuit pathways;

symmetrically distributing a clock signal to the plurality of data conversion circuits along a plurality of symmetrical clock circuit pathways, wherein clock transmission times associated with each clock circuit pathway are substantially equal, and wherein the symmetrical data circuit pathways are symmetrical relative to the symmetrical clock circuit pathways; and

latching data at the data conversion circuits from the first plurality of bit streams with the distributed clock signal to produce the second bit stream.

13. The method of Claim 12, further comprising the steps of:

delaying the distributed clock signal within individual symmetrical clock circuit pathways to compensate for skewing of the data clock signal received by each data conversion circuit; and

retiming data at the individual data conversion circuits to compensate for skewing of data within the first bit streams received by each data conversion circuit.

14. The method of Claim 13, wherein delaying the distributed clock signal further comprises introducing delay elements with switched capacitor networks.

15. The method of Claim 13, wherein retiming data further comprises introducing delay elements with switched capacitor networks.

16. The method of Claim 14, wherein the switched capacitor networks provide a controlled variable capacitance.

17. The method of Claim 16, wherein the data conversion circuits comprise a multiplexer, wherein a number of first bit streams exceeds a number of second bit streams, and wherein the second data rate exceeds the first data rate.

18. The method of Claim 17, wherein the first bit streams comprise 4 bit streams at about 10GBPS, and wherein the second bit streams comprise 1 bit stream at about 40 GBPS.

19. The method of Claim 17, wherein the first bit streams comprise 16 bit streams at about 2.5 GBPS, and wherein the second bit streams comprise 4 bit streams at about 10 GBPS.

20. The method of Claim 17, wherein a physical length of each symmetrical data circuit pathway is substantially equal, and wherein a physical length of each symmetrical clock circuit pathway is substantially equal.

21. A multistage bit stream multiplexer, comprising:

a first multiplexing integrated circuit that receives a first plurality of bit streams at a first bit rate and that produces a second plurality of bit streams at a second bit rate, wherein the first plurality of bit streams are greater in number than the second plurality of bit streams are in number, and wherein the first bit rate is less than the second bit rate;

a clock circuit, wherein the clock circuit generates a forward data clock;

a plurality of symmetrical data circuit pathways that transport the second plurality of bit streams from the first multiplexing integrated circuit;

a second multiplexing integrated circuit that receives the second plurality of bit streams from the plurality of symmetrical data pathways, wherein a transmission time for the second plurality of bit streams on the plurality of symmetrical data circuit pathways are substantially equal, and wherein the second multiplexing integrated circuit receives the forward data clock and symmetrically distributes the forward data clock signal along a plurality of symmetrical clock circuit pathways, wherein clock transmission times associated with each clock circuit pathway are substantially equal, and wherein the distributed data clock signal latches data from the second plurality of bit streams to produce a high speed bit stream.

22. The multistage bit stream multiplexer of Claim 21, wherein the symmetrical clock circuit pathways further comprises delay elements operable to compensate for skewing of the forward data clock signal.

23. The multistage bit stream multiplexer of Claim 22, wherein the delay elements comprise switched capacitor networks that introduce delay increments based on a capacitance coupled to a buffer amplifier.

24. The multistage bit stream multiplexer of Claim 23, wherein the capacitance coupled to the buffer amplifier is a variable capacitance.

25. The multistage bit stream multiplexer of Claim 24, wherein each symmetrical data circuit pathways further comprises a retimer that ensures data integrity between the second plurality of bit streams and the high speed bit stream.

26. A multistage bit stream demultiplexer, comprising:

a first demultiplexing integrated circuit that receives a first plurality of bit streams at a first bit rate and that produces a second plurality of bit streams at a second bit rate, wherein the second plurality of bit streams are greater in number than the first plurality of bit streams are in number, and wherein the first bit rate exceeds the second bit rate;

a clock circuit, wherein the clock circuit generates a forward data clock;

a plurality of symmetrical data circuit pathways that transport the second plurality of bit streams from the first demultiplexing integrated circuit;

a second demultiplexing integrated circuit that receives the second plurality of bit streams from the plurality of symmetrical data pathways, wherein transmission times for the second plurality of bit streams on the plurality of symmetrical data circuit pathways are substantially equal, and wherein the second demultiplexing integrated circuit receives

the forward data clock and symmetrically distributes the forward data clock signal along a plurality of symmetrical clock circuit pathways, wherein clock transmission times associated with each clock circuit pathway are substantially equal, and wherein the distributed data clock signal latches data from the second plurality of bit streams to produce a low speed bit stream.

27. The multistage bit stream demultiplexer of Claim 26, wherein the symmetrical clock circuit pathways further comprises delay elements operable to compensate for skewing of the forward data clock signal.

28. The multistage bit stream demultiplexer of Claim 27, wherein the delay elements comprise switched capacitor networks that introduce delay increments based on a capacitance coupled to a buffer amplifier.

29. The multistage bit stream demultiplexer of Claim 28, wherein the capacitance coupled to the buffer amplifier is a variable capacitance.

30. The multistage bit stream demultiplexer of Claim 29, wherein each symmetrical data circuit pathways further comprises a retimer that ensures data integrity between the second plurality of bit streams and the low speed bit stream.